Appl. No. 09/837,022

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit:	2827
Attorney Docket No.:	121056-020
Applicant:	Hiroshi KIMURA
Invention:	SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAME
Serial No:	09/837,022
Filed:	April 18, 2001
Examiner:	James Mitchell

RESPONSE AFTER FINAL REJECTION

EXPEDITED PROCESSING REQUESTED

Certificate Under 37 CFR 1.8(b)

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office via facsimile transmission on the date indicated below.

on December 18, 2003

Michael S. Gzybowski

DECLARATION BY MR. HIROSHI KIMURA SUBMITTED UNDER 37 CFR §1.132

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Hiroshi KIMURA, hereby declare and say as follows:

1. I am currently employed as the director of the Management Division Package Technical Department of Torex Semiconductor Ltd. In my present position I am responsible for unifying the development, design and mass production of semiconductor packages for my company's manufacturing line.

2. That my educational background includes four (4) years of studying Material Engineering in the Applied Chemical course in the Engineering Department of Toyo University.

3. That after completing my study at the Engineering Department of Toyo University I became employed by Torex Semiconductor Ltd. where I have researched electric/electronic materials and have been engaged with the production of resin-packaged products for twenty (20) years.

4. That I am the inventor of U.S. Patent Application Serial No. 09/837,022 and am familiar with the pending specification and claims.

5. That I am familiar with the Office Action mailed July 1, 2003 in U.S. Patent Application Serial No. 09/837,022.

6. That I am familiar with the prior art references cited and relied upon by Examiner James Mitchell in Office Action mailed July 1, 2003 in U.S. Patent Application Serial No. 09/837,022 and particularly with U.S. Patent Application Publication No. 2002/0100165 to Glenn.

7. That electroforming techniques (Electro-Casting or Electrodeposition) have been generally applied to ornaments, but have not been applied to the field of electronic products, so that such techniques are not familiar to those in the field of electronic products.

8. That in the invention set forth and claimed in U.S. Patent Application Serial No. 09/837,022 the application of electrodeposition does not produce an alloy between the metallic substrate and the metallic layer 8. Accordingly, the metal substrate 9 can be easily removed form the resin sealing body 11.

9. That, since removal of the metal substrate 9 from the resin sealing body 11 before the steps of wiring and resin sealing cannot lead to the production of semiconductor devices, the contact strength between the metallic substrate and the metallic layer must be maintained.

10. That in the case of metallic substrates, the contact strength can be adjusted by suitably etching the surface of the metallic substrate before electrodeposition of the metallic layer.

11. That using electrodeposition for making a lead frame and using related techniques such as etching to provide a suitable contact strength between a metallic substrate and a metallic layer are techniques that belong to a different technical field than the techniques of applying a metal layer to a plastic substrate.

12. That therefore, it follows that one of ordinary skill in the art reading Glenn would avoid using and metal substrate and would not consider of replacing the plastic substrate of Glenn with a metal substrate.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date Signature

105192.1